What is clamed is:

1. An organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

2. An organic insulating film according to Claim 1, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

3. An organic insulating film according to Claim 1, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

4. An organic insulating film according to Claim 3, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

5. An organic insulating film according to Claim 1, wherein a C=C bond is contained.

6. An organic insulating film according to Claim 5, wherein a vinyl group is contained.

7. An organic insulating film according to one of Claims 1, wherein

said organic insulating film is one selected from the group consisting of a SiCH film, a SiCHN film and a SiOCH film.

8. An organic insulating film according to Claim 7, wherein said SiCH film is composed of Si, C and H elements and a C/Si composition ratio thereof is not less than 0.9.

9. An organic insulating film according to Claim 8, wherein said SiCH film has a density of less than 1.4 g / cm^3.

10. An organic insulating film according to Claim 7, wherein said SiCHN film is composed of Si, C, H and N elements and a C/Si composition ratio thereof is not less than 1.0.

11. An organic insulating film according to Claim 10, wherein said SiCHN film has a density of less than 1.6 g / cm^3.

12. An organic insulating film according to Claim 7, wherein said SiOCH film is composed of, at least, Si, C, O and H elements and a C/Si composition ratio thereof is not less than 0.8.

13. An organic insulating film according to Claim 12, wherein said SiOCH film has a density of less than 1.2 g / cm^3.

14. A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD (Chemical Vapor Deposition) method, and source gases are an oxidizing agent, an inert gas and a polyorganosilane

whose C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

15. A method of manufacturing an organic insulating film according to Claim 14, wherein said inert gas is one selected from the group consisting of helium, argon and xenon.

16. A method of manufacturing an organic insulating film according to Claim 14, wherein said oxidizing agent is one selected from the group consisting of O_2, O_3, H_2O, CO and CO_2.

17. A method of manufacturing an organic insulating film according to Claim 14, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

18. A method of manufacturing an organic insulating film according to Claim 14, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

19. A method of manufacturing an organic insulating film according to Claim 18, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

20. A method of manufacturing an organic insulating film according to Claim 14, wherein said organic insulating film is a SiOCH film composed of, at least, Si, C, H and O elements.

21. A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD method, and source gases are an inert gas that is one of helium, argon and xenon, and an polyorganosilane whose C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

22. A method of manufacturing an organic insulating film according to Claim 21, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

23. A method of manufacturing an organic insulating film according to Claim 21, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

24. A method of manufacturing an organic insulating film according to Claim 23, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

25. A method of manufacturing an organic insulating film according to

Claim 21, wherein said organic insulating film is a SiCH film composed of Si, C and H elements.

26. A method of manufacturing an organic insulating film, wherein a film is grown by the plasma CVD method, and source gases are a nitrogen containing gas, an inert gas that is one of helium, argon and xenon, and an polyorganosilane whose C/Si ratio is, at least, equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

27. A method of manufacturing an organic insulating film, wherein said nitrogen containing gas is one of ammonia, N_2 and hydrazine.

28. A method of manufacturing an organic insulating film according to Claim 26, wherein said polyorganosilane is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane, tetravinylsilane, tetraethylsilane and triethylsilane.

29. A method of manufacturing an organic insulating film according to Claim 26, wherein said polyorganosilane contains a vinyl group, at least, in a part thereof.

30. A method of manufacturing an organic insulating film according to Claim 29, wherein said polyorganosilane containing a vinyl group, at least, in a part thereof is one or more types of polyorganosilanes selected from the group consisting of trimethylvinylsilane, triethlvinylsilane, dimethyldivinylsilane, diethyldivinylsilane, methyltrivinylsilane, ethyltrivinylsilane and tetravinylsilane.

31. A method of manufacturing an organic insulating film according to Claim 26, wherein said organic insulating film is a SiCHN film composed of Si, C, H and N elements.

32. A semiconductor device comprising, at least, one insulating film selected from the group consisting of an interlayer insulating film, an etching stopper film and a barrier insulating film against a metal; wherein

said interlayer insulating film, etching stopper film or barrier insulating film against a metal is an organic insulating film; wherein

said organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

33. A semiconductor device according to Claim 32, which comprises a trench interconnection structure.

34. A semiconductor device having a trench interconnection structure, which comprises a first insulating film formed on a semiconductor substrate, a first trench interconnection formed in said first insulating film, a second insulating film, a third insulating film, a second trench interconnection formed in said third insulating film, a via plug that is formed in said second insulating film and connects said first trench interconnection with said second trench interconnection; wherein

at least said first insulating film, said second insulating film and said third insulating film are each made of a SiOCH film as set forth in Claim7.

35. A semiconductor device according to Claim 34, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

36. A semiconductor device according to Claim 34; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

37. A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film, a SiOCH film as set forth in Claim 7 and a hard mask film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

38. A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

39. A semiconductor device according to Claim 34; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

40. A semiconductor device according to Claim 34, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

41. A semiconductor device according to Claim 34; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

42. A semiconductor device according to Claim 34; wherein

a top section of said second trench interconnection is covered with a barrier insulating film; and

said barrier insulating film is either of a SiCH film and a SiCHN film as set forth in Claim 7.

43. A semiconductor device according to one of Claims 36, 39 and 41, wherein said etching stopper film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

44. A semiconductor device according to one of Claims 37, 38, 39 and 42, wherein said barrier insulating film is a layered film made of a SiCH film and a SiCHN film as set forth in Claim 7.

45. A semiconductor device according to Claim 34, wherein, at least, one of said trench interconnection and said via plug is formed of a copper containing metal.

46. A semiconductor device according to Claim 45, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

47. A semiconductor device according to Claim 34, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

48. A method of manufacturing a semiconductor device which comprises, at least, one insulating film selected from the group consisting of an interlayer insulating film, an etching stopper film and a barrier insulating film against a metal; wherein

said interlayer insulating film, etching stopper film or barrier insulating film against a metal is an organic insulating film ;wherein

said organic insulating film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100 ;wherein

said organic insulating film is one selected from the group consisting of a SiCH film, a SiCHN film and a SiOCH film.

49. A method of manufacturing a semiconductor device according to Claim 48, wherein said semiconductor device comprises a trench interconnection structure.

50. A method of manufacturing a semiconductor device having a

trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film;

etching said second insulating film selectively and thereby forming a via hole to reach the top face of said first trench interconnection;

filling up said via hole with a metal to form a via plug;

forming a third insulating film;

etching said third insulating film selectively and thereby forming a second interconnection trench pattern so that at least a part thereof may reach the top face of said via plug;

filling up said second interconnection trench pattern with a metal to form a second trench interconnection; and

forming a barrier insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

51. A method of manufacturing a semiconductor device according to Claim 50, wherein

said first insulating film is a layered film made of said SiOCH film and a hard mask film.

52. A method of manufacturing a semiconductor device according to Claim 50; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of said SiCH film and said SiCHN film; wherein

said SiCH and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

53. A method of manufacturing a semiconductor device according to Claim 50; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and a hard mask film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

54. A method of manufacturing a semiconductor device according to Claim 50, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

55. A method of manufacturing a semiconductor device according to Claim 50; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

56. A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film and a third insulating film;

etching said second insulating film and said third insulating film selectively and thereby forming a via hole to reach the top face of said first insulating film;

etching said third insulating film selectively and thereby forming a second interconnection trench to reach the top face of said second insulating film;

filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

57. A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film and a third insulating film;

etching said third insulating film selectively and thereby forming a second interconnection trench to reach the top face of said second insulating film;

etching a part of a bottom section of said second interconnection trench selectively and thereby forming a via hole to reach the top face of said first insulating film;

filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film; wherein

said SiOCH film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

58. A method of manufacturing a semiconductor device according to Claim 56, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

59. A method of manufacturing a semiconductor device according to Claim 57, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

60. A method of manufacturing a semiconductor device according to Claim 56; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film: wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

61. A method of manufacturing a semiconductor device according to Claim 57; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film: wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

62. A method of manufacturing a semiconductor device according to Claim 56; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

63. A method of manufacturing a semiconductor device according to Claim 57; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

64. A method of manufacturing a semiconductor device according to Claim 56; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film ; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

65. A method of manufacturing a semiconductor device according to Claim 57; wherein

said second insulating film is a layered film made of a barrier insulating film, said SiOCH film and an etching stopper film; and

each of said barrier insulating film and said etching stopper film is either of a SiCH film and a SiCHN film ; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

66. A method of manufacturing a semiconductor device according to Claim 56, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

67. A method of manufacturing a semiconductor device according to Claim 57, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

68. A method of manufacturing a semiconductor device according to Claim 56; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film;

wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

69. A method of manufacturing a semiconductor device according to Claim 57; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

70. A method of manufacturing a semiconductor device having a trench interconnection structure; which comprises the steps of:

forming a first insulating film on a semiconductor substrate;

etching said first insulating film selectively and thereby forming a first interconnection trench pattern;

filling up said first interconnection trench pattern with a metal to form a first trench interconnection;

forming a second insulating film;

forming an etching stopper film;

making an opening selectively in said etching stopper film;

forming a third insulating film;

etching said third insulating film selectively so that a second

interconnection trench to reach the top face of said second insulating film may be formed and, together therewith, forming a via hole to reach a top section of said first interconnection through said opening;

filling up said via hole and said second interconnection trench with a metal to form a via plug and a second trench interconnection; and

forming a fourth insulating film; wherein

at least one insulating film selected from the group consisting of said first, second and third insulating films is made of a SiOCH film, and said etching stopper film is made of either of a SiCH film and a SiCHN film ; wherein

said SiOCH film, said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

71. A method of manufacturing a semiconductor device according to Claim 70, wherein said first insulating film is a layered film made of said SiOCH film and a hard mask film.

72. A method of manufacturing a semiconductor device according to Claim 70; wherein

said first insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

73. A method of manufacturing a semiconductor device according to Claim 70; wherein

said second insulating film is a layered film made of a barrier insulating film and said SiOCH film; and

said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

74. A method of manufacturing a semiconductor device according to Claim 70, wherein said third insulating film is a layered film made of said SiOCH film and a hard mask film.

75. A method of manufacturing a semiconductor device according to Claim 70; wherein

said third insulating film is a layered film made of an etching stopper film, said SiOCH film and a hard mask film; and

said etching stopper film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

76. A method of manufacturing a semiconductor device according to Claim 70; wherein said barrier insulating film is either of a SiCH film and a SiCHN film; wherein

said SiCH film and said SiCHN film formed using, as a source, a polyorganosilane whose C/Si ratio is at least equal to or greater than 5 and, at the same time, molecular weight is equal to or greater than 100.

77. A method of manufacturing a semiconductor device according to Claim 50, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

78. A method of manufacturing a semiconductor device according to one of Claims 50, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

79. A method of manufacturing a semiconductor device according to one of Claims 50, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

80. A method of manufacturing a semiconductor device according to Claim 56, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

81. A method of manufacturing a semiconductor device according to one of Claims 56, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

82. A method of manufacturing a semiconductor device according to one of Claims 57, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

83. A method of manufacturing a semiconductor device according to Claim 57, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

84. A method of manufacturing a semiconductor device according to one of Claims 57, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

85. A method of manufacturing a semiconductor device according to one of Claims 57, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.

86. A method of manufacturing a semiconductor device according to Claim 64, wherein at least one of said trench interconnection and said via plug is formed of a copper containing metal.

87. A method of manufacturing a semiconductor device according to one of Claims 64, wherein said copper containing metal further contains one or more metals selected from the group consisting of Si, Al, Ag, W, Mg, Be, Zn, Pd, Cd, Au, Hg, Pt, Zr, Ti, Sn, Ni and Fe.

88. A method of manufacturing a semiconductor device according to one of Claims 64, wherein said trench interconnection and said via plug each comprise one or more barrier metal layers selected from the group consisting of layers of Ti, TiN, TiSiN, Ta, TaN and TaSiN.